**Chapter 7**

1. Draw the logic diagram, logic symbol and truth table for the active LOW input - latch.

2. Draw the logic diagram, logic symbol and truth table for the active HIGH input - latch.

3. Determine the Q output of an active-LOW input - latch if the waveforms in Figure.



4. Draw the logic diagram, logic symbol and truth table for the gated S-R latch.

5. Determine the *Q* output waveform if the inputs shown in Figure are applied to a gated S-R latch that is

initially RESET.



6. Determine the *Q* output waveform if the inputs shown in Figure are applied to a gated D latch, which is

initially RESET.



7. Draw the logic diagram, logic symbol and truth table for J-K flip flop.

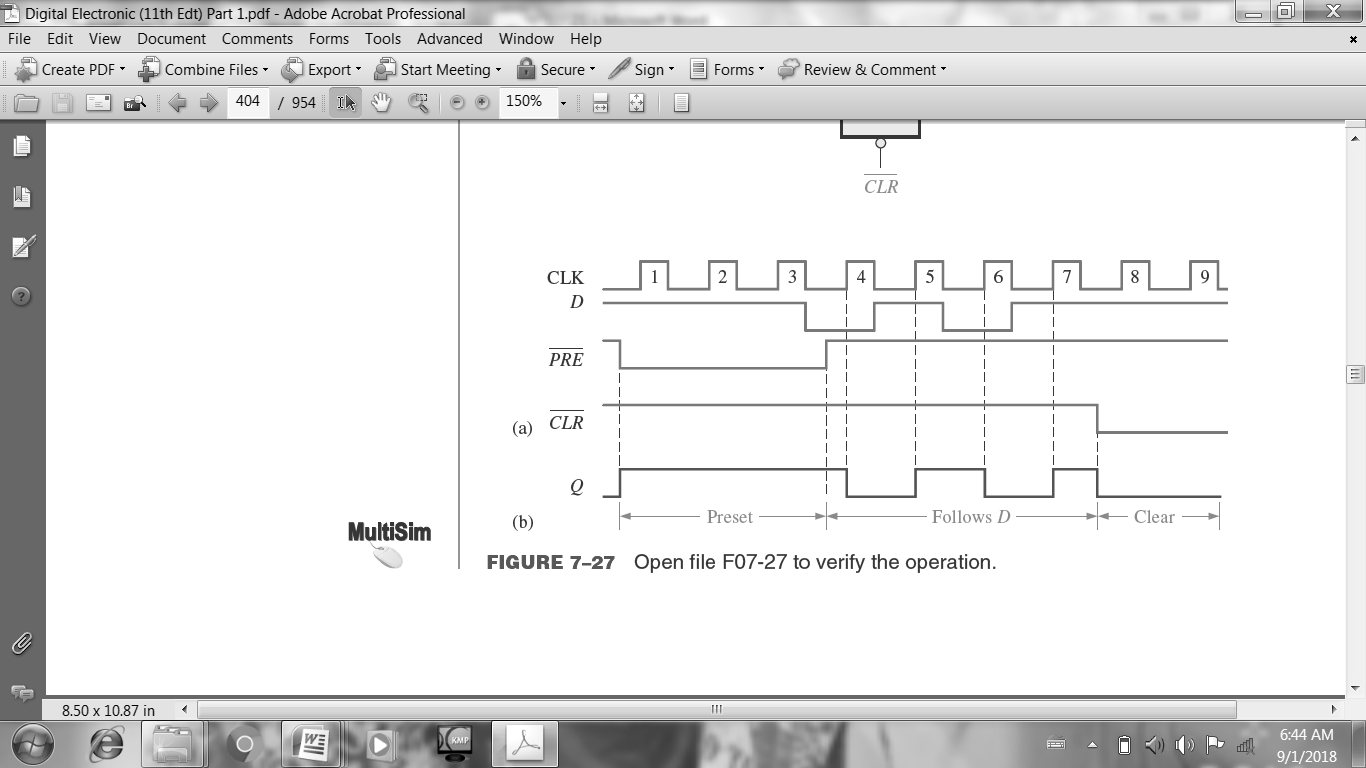
8. Draw the Q outputs for the positive and negative edge triggered J-K flip-flops. The J, K and clock input

are shown in Figure. Assume Q outputs are initially LOW.



9. For the positive edge-triggered D flip-flop with preset and clear inputs in figure, determine the Q output

for the following timing diagram if *Q* is initially LOW.



10. For the positive edge triggered D flip-flop which is one part of 74HC74 with preset and clear input in Figure, determine the Q output if Q is RESET.



11. The 1J, 1K, 1CLK, 1PRE, and 1CLR waveforms in Figure are applied to one of the negative edge-

triggered flip-flops in a 74HC112 package. Determine the 1Q output waveform.



12. The 2J, 2K, 2CLK, 2PRE and 2CLR waveforms in figure are applied to one of the negative edge-triggered flip flop in a 74HC112 package. Determine the 2Q output waveform.



13. Draw the internal functional diagram of a 555 timer with pin numbers. And then, name the two modes which it can be used.

14. A 555 timer is configured to run as multivibrator as shown in figure. Determine its frequency and duty cycle. If a diode is connected across R2, determine the duty cycle.



15. Determine the value of REXT that will produce a pulse width of 5µs when connected to a 74LS122. Show

the connections. Assume CEXT = 560 pF.

16. An output pulse of 100 ms duration is to be generated by a 74121 one-shot. Using a capacitor of 3.3 µF,

determine the value of external resistance required.

17. Determine the values of the external resistors for a 555 timer used as an astable multivibrator with an

output frequency of 10 kHz, if the external capacitor C is 0.004µF and the duty cycle is to be approximately 80%.

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**Chapter 8**

1. Sketch the basic data movement in 4-bit shift register.

2. Sketch the 4-bit Serial-in-Serial-out shift register circuit and logic symbol.

3. Sketch the 4-bit Serial-in-Parallel-out shift register circuit and logic symbol.

4. Sketch the 4-bit Parallel -in-Parallel-out shift register circuit and logic symbol.

5. Show the states of the 5-bit register in Figure for the specified data input and clock waveforms. Assume

that the register is initially cleared (all 0s).



6. Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms in Figure. The

register initially contains all 1s.

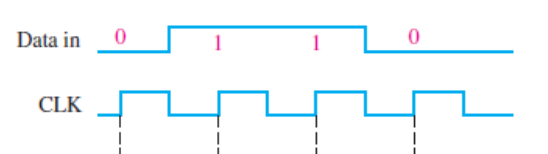
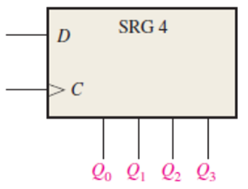
  
7. Develop the Q0 through Q7 outputs for a 74HC164 shift register with the input waveforms shown in

Figure.



**OR**



8. Determine all the *Q* output waveforms for a 74HC195 4-bit shift register when the inputs are as shown in

Figure.



**OR**



9. Determine the Q outputs of a 74HC194 with the inputs shown in Figure. InputsD0, D1, D2 and D3 are

all HIGH.



**OR**

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10. Determine the Q outputs of a 74HC194 with the inputs shown in Figure.



11. Use 74HC195 4-bit shift registers to create an 8-bit shift register. Show the connections.

12. Use two 74HC194 4-bit bidirectional shift registers to create an 8-bit bidirectional shift register. Show

the connections.

13. Use two 74HC194 4-bit bidirectional shift registers to create a 12-bit bidirectional shift register. Show

the connections.

14. Use 74HC195 4-bit shift registers to implement a 12-bit ring counter. Show the connections.

15. Use 74HC195 4-bit shift registers to implement a 16-bit ring counter. Show the connections.

16. Determine the stage of the shift register of figure after each clock pulse for the given RIGHT/

control input waveform. Assume that Q0= 1, Q1=0, Q2= 1 and Q3= 1 and that the serial data input line is

HIGH.



17. For the 8-bit bidirectional register in figure, determine the state of the register after each clock pulse for

the RIGHT/control waveform given. A HIGH on this input enables a shift to right, and a LOW

enables a shift to the left. Assume that the register is initially storing the decimal number forty three in

binary, with the right most position being the LSB. There is a LOW on the data input line.



18. Determine the amount of time delay between the serial input and each output in figure.



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**Chapter 9**

1. Sketch the 4-bit asynchronous binary counter circuit. Each flip flop is negative edge trigger and propagation delay of 10 ns. Draw the timing diagram and determine the total propagation delay time and maximum clock fequency.

2. Sketch the asynchronous decade counter and then draw the timing diagram and state the truth-table.

Assume the counter operates negative edge trigger.

**OR**

Draw an asynchronous decade counter, state sequence and timing diagram.

3. Show how an asynchronous counter can be implemented having a modulus-12 with a straight binary sequence from 0000 through 1011. Assume the counter operates negative edge trigger.

4. Show how an asynchronous counter can be implemented a modulus-13 with a straight binary sequence

from 0000 through 1100. Assume the counter operates negative edges trigger.

**OR**

Design an asynchronous counter using J-K flip flops having a modulus of 13 and other logic gates.

5. Show how an asynchronous counter can be implemented a modulus-14 with a straight binary sequence

from 0000 through 1101. Assume the counter operates negative edge trigger.

6. Draw the timing diagram and determine the sequence of a 4-bit synchronous binary up/down counter if

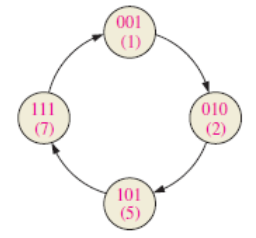
the clock and UP/DOWN control inputs waveforms as shown in Figure. The counter starts in the all 0s

state and is positive edge-trigger.



7. Design a counter with the irregular binary count sequence shown in the state diagram of Figure. Use D

flip-flops.



8. Design a counter with the irregular binary count sequence shown in the state diagram of Figure. Use J-K

flip-flops.



9. Develop a synchronous 3-bit up/down counter with Gray code sequence using J-K flip-flops. The counter should count up when an UP/DOWN control input is 1 and count down when the control input is 0.



10. Use 74HC190 up/down decade counters connected in the DOWN mode to obtain a 10 kHz waveform

from a 1 MHz clock. Show the logic diagram.

11. Design a counter to produce the following binary sequence. Use J-K flip-flops.

0,2,1,3,0,… or 00, 10, 01, 11, 00, …

12. Design a counter to produce the following binary sequence. Use J-K flip-flops.

1, 4, 3, 5, 7, 6, 2, 1, …

13. The following clock and clear waveforms in Figure are used as input waveforms to a BCD decade counter. Determine the waveforms for each the counter outputs (Q0, Q1, Q2 and Q3). The clear is synchronous, and the counter is initially the binary 0110.



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**Chapter 12**

1. What does sampling mean?

2. Illustrate the sampling process with figure.

3. Explain what the followings are: Sampling, Nyquist frequency, Quantization, Aliasing, and Digital to

analog converter.

4. Determine the binary code output of the 3-bit flash ADC in figure for the input signal and the encoder

enable pulses shown. For this example, VREF = +8 V.



5. Draw the simplified block diagram of a digital cellular phone.

6. Determine the output of the DAC for figure in part (a) if the sequence of the 4-bit numbers in part (b) is

applied to the inputs. The data inputs have a LOW value of 0V and a HIGH value of +5V.



**OR**



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Fill in the blank.

**Chapter 7**

1. A latch has two stable states.

2. A latch is considered to be in the RESET state when the *Q* output is low.

3. A feature that distinguishes the J-K flip-flop from the D flip-flop is toggle condition.

4. Flip-flops and latches are both bistable devices.

5. A clock input is necessary for an edge-triggered flip-flop.

6. When the *J* and *K* inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.

7. A one-shot is also known as a monostable multivibrator.

8. When triggered, a one-shot produces a single pulse.

9. Anstable multivibrator is also known as a pulse oscillator.

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**Chapter 8**

1. Shift registers consist of an arrangement of flip-flops.

2. Storage and data movement are two functions of a shift register.

3. A serial shift register accepts one bit at a time on a single line.

4. With a 100 kHz clock frequency, eight bits can be serially entered into a shift register in 80 ms.

5. A shift register counter is a shift register with the serial output connected back to the serial input.

6. A shift register with four stages can store a maximum count of fifteen.

7. When an 8-bit serial in/serial out shift register is use for a 24 µs time delay, the clock frequency must be

333 kHz.

8. The modulus of an 8-bit Johnson counter requires four flip-flops.

9. The modulus of an 8-bit ring counter requires eight flip-flops.

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**Chapter 9**

1. Two basic types of state machines are Moore and Mealy.

2. A Moore state machine consists of combinational logic circuit that determines the sequence and memory.

3. The output of a Mealy machine depends on its inputs and present state.

4. An asynchronous counter is also known as a ripple counter.

5. A decade counter has ten states.

6. A counter with four stages has a maximum modulus of sixteen.

7. To achieve a maximum modulus of 32, sixteen stages are required.

8. If the present state is 1000, the next state of a 4-bit up/down counter in the DOWN mode is 0111.

9. A 4-bit binary up/down counter is in the binary state of zero (0000). The next state in the DOWN mode is

1111.

10. A decade counter with a count of zero (0000) through nine (1001) is known as a BCD counter.

11. Three cascaded modulus-10 counters have an overall modulus of 1000.

**Chapter 12**

1. An analog signal can be converted to a digital signal using sampling.

2. An ADC is an analog to digital converter.

3. A DAC is a digital-to-analog converter.

4. An op-amp is a linear amplifier which has two inputs and one output.

5. A digital voltmeter uses a dual-slope ADC.

6. If the highest frequency component in an analog signal is 20 kHz, the minimum sample frequency is 40

kHz.

7. A 4-bit flash ADC requires fifteen comparators.

8. Delta modulation is based on the difference of two successive samples.

9. Two types of DAC are binary-weighted input and R/2R ladder.

10. The process of converting an analog value to a code is called quantization.

11. The quantization process converts the sample-and-hold output to binary code.

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